

Corrected
10672927**Accumulator for Adaptive Sigma-Delta Modulation****Cross Reference to Related Applications**

The present application is a continuation-in-part of U.S. Patent Application 10/109,537, filed on March 28, 2002, which is now a U.S. Patent 6,661,363. This application is also a continuation-in-part of U.S. Patent Application No. 10/357,613, filed on February 4, 2003, which is now a U.S. Patent 6,727,833. This application is a continuation of U.S. Patent Application No. 09/496,756, filed February 3, 2000, which issued as U.S. Patent 6,535,153 and claims priority from U.S. provisional application number 60/118,607, filed February 4, 1999. Each of the above-mentioned applications is hereby incorporated herein by reference.

Technical Field

The invention generally relates to signal processing, and more particularly, to analog to digital conversion using sigma-delta modulation.

Background Art

Sigma-delta (Σ - Δ) modulation is a widely used and thoroughly investigated technique for converting an analog signal into a high-frequency digital sequence. See, for example, "Oversampling Delta-Sigma Data Converters," eds. J. C. Candy and G. C. Temes, IEEE Press, 1992, (hereinafter Candy) and "Delta-Sigma Data Converters," eds. S. R. Northworthy, R. Schreier, G. C. Temes, IEEE Press, 1997, both of which are hereby incorporated herein by reference.

In Σ - Δ modulation, a low-resolution quantizer is incorporated within a feedback loop configuration in which the sampling frequency is much higher than the Nyquist frequency of the input signal (i.e., much higher than twice the maximum input frequency). In addition, the noise energy introduced in the quantizer is shaped towards higher frequencies according to a so called "noise-transfer-function" $NTF(z)$, and the signal passes the modulator more or less unchanged according to a so called "signal-transfer-function" $STF(z)$.

Fig. 1(a) depicts a simple first order Σ - Δ modulator for a discrete time system having a subtraction stage 101, an accumulator 102 (including an integrator adder 103 and a delay line 104), a one-bit quantizer 105, and a 1-bit digital-to-analog converter